Abstract of the Disclosure

An integrated circuit including at least one loop filter for use in a phase-locked loop, the loop filter including a resistive element and at least one metal-oxide-semiconductor (MOS) transistor configured as a capacitor having a first capacitance associated therewith. The MOS transistor is connected between a voltage source and an input of the loop filter via the resistive element. The loop filter further includes a bias circuit connected to the MOS transistor. The bias circuit is configured for maintaining a substantially constant reference voltage across the MOS transistor, the reference voltage being selected so as to bias the MOS transistor in a designated region of operation. In this manner, the first capacitance is substantially optimized per unit area.